

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Chen *et al.*

Appl. No.: *To Be Assigned*

Filed: *Herewith*

For: **System and Method for One-Time
Programmed Memory Through
Direct-Tunneling Oxide Breakdown**

Confirmation No.: *To Be Assigned*

Art Unit: *To Be Assigned*

Examiner: *To Be Assigned*

Atty. Docket: 1875.0220001

Information Disclosure Statement

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Applicant has listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application

does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

In accordance with 37 C.F.R. § 1.97(b), this Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

No copies of U.S. patents and patent application publications cited on the attached Form PTO-1449 are submitted in accordance with 1276 OG 55 because this application was filed after June 30, 2003.

Copies of cited documents AR1, AS1, AT1, AR2 and AS2 are submitted herewith.

It is expected that the Examiner will review the prosecution and cited art in the parent application no. 09/739,752, filed December 20, 2000, in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

Chen *et al.*
Appl. No. *To Be Assigned*

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.0220001	APPLICATION NO. To Be Assigned
	FIRST NAMED INVENTOR Vincent Chen	
	FILING DATE Herewith	ART UNIT To Be Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA1	4,173,791	11/1979	Bell, Antony G.			
	AB1	4,499,557	02/1985	Holmberg <i>et al.</i>			
	AC1	5,163,180	11/1992	Eltoukhy <i>et al.</i>			
	AD1	5,480,828	01/1996	Hsu <i>et al.</i>			
	AE1	5,742,555	04/1998	Marr <i>et al.</i>			
	AF1	5,748,025	05/1998	Ng <i>et al.</i>			
	AG1	5,834,824	11/1998	Shepherd <i>et al.</i>			
	AH1	5,886,392	03/1999	Schuegraf			
	AI1	5,949,712	09/1999	Rao <i>et al.</i>			
	AJ1	6,044,012	03/2000	Rao <i>et al.</i>			
	AK1	6,096,580	08/2000	Iyer <i>et al.</i>			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	1	Clark, Lawrence T., "A High-Voltage Output Buffer Fabricated on a 2V CMOS Technology," <i>Symposium on VLSI Circuits Digest of Technical Papers</i> , pp. 61-62, 1999.
	AS	1	International Search Report for PCT/US01/48853, 5 pages, July 31, 2002.
	AT	1	Schroder, Dieter K., "Semiconductor Material and Device Characterization," Fig. E6.5(a), Oxide failure modes, John Wiley & Sons, Inc., 2 nd Edition, p. 391, 1998.

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	6,096,610	08/2000	Alavi <i>et al.</i>			
	AB2	6,184,726 B1	02/2001	Haeberli <i>et al.</i>			06/29/1999
	AC2	6,266,269 B1	07/2001	Karp <i>et al.</i>			06/07/2000
	AD2	6,351,425 B1	02/2002	Porter, Stephen R.			12/07/2000
	AE2	6,477,094 B2	11/2002	Kim <i>et al.</i>			12/18/2000
	AF2	6,549,458 B1	04/2003	Rao <i>et al.</i>			10/25/2001
	AG2						
	AH2						
	AI2						
	AJ2						
	AK2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	2	Schroder, Dieter K., "Semiconductor Material and Device Characterization," Fig. 6.40, Charge-to-breakdown as a function of oxide thickness, John Wiley & Sons, Inc., 2 nd Edition, p. 397, 1998.
	AS	2	Shi, Y., <i>et al.</i> , "Polarity-Dependent Tunneling Current and Oxide Breakdown in Dual-Gate CMOSFET's," <i>IEEE Electron Device Letters</i> , Volume 19, No. 10, pp. 391-393, October 1998.
	AT	2	

EXAMINER

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